



Formal Methods and Models for System Design: A System Level Perspective

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Perhaps nothing characterizes the inherent heterogeneity in embedded systems than the ability to choose between hardware and software implementations of a given system function. Indeed, most embedded systems at their core represent a careful division and design of hardware and software parts of the system. To do this task effectively, models and methods are necessary functionality. To capture application behavior, needs and system implementation constraints. Formal modeling can be valuable in addressing these tasks. As with most engineering domains, co-design practice defines the state of the art. It seeks to add new capabilities in system conceptualization, modeling, optimization and implementation. These advances - particularly those related to synthesis and verification tasks - directly depend upon formal understanding of system behavior and performance measures. Current practice in system modeling relies upon exploiting high-level programming frameworks, such as SystemC, Esterel, to capture design at increasingly higher levels of abstraction and attempts to reduce the system implementation task. While raising the abstraction levels for design and verification tasks, to be really useful, these approaches must also provide for reuse, adaptation of the existing intellectual property (IP) blocks.

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